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Review of Gates in Digital Electronics

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Abstract: **Digital Electronics is the back bone of current world due to integrated circuit fabrications process, electronic circuits includes very complex embedded digital block as serial receivers. Here, in this paper we will be discussing about various gates and their applications with which they made our life easier. We will also be discussing about half adder, full adder, half sub-tractor and full sub-tractor which are made with the help of simple basic gate. No doubt digital electronics has made our life much easier, though we may not see it but it does play a major role.**

Logic gates

1. INTRODUCTION

A **Digital Logic Gate** is an electronic device implementing Boolean function that makes logical decisions based on the different combinations of digital signals present on its inputs. Digital logic gates may have more than one input but generally only have one digital output. Individual logic gates can be connected together to form combinational or sequential circuits or larger logic gate functions**.** They are primarily implemented using diodes or transistors acting as electronic switches, but can also be constructed using electromagnetic relays (relay logic), fluidic logic, pneumatic logic, optics, molecules, or even mechanical elements. With amplification, logic gates can be cascaded in the same way that Boolean functions can be composed, allowing the construction of a physical model of all of Boolean logic, and therefore, all of the algorithms and mathematics that can be described with Boolean logic. Logic circuits include such devices as multiplexers, registers, arithmetic logic units (ALUs), and computer memory, all the way up

Through complete microprocessors, this may contain more than 100 million gates. In practice, the gates are made from field-effect transistors (FETs), particularly MOSFETs (metal–oxide–Semiconductor field-effect transistors).

Digital logic gates are available in two basic forms:
a. TTL
b. CMOS

a. TTL (*Transistor-Transistor Logic) i.e. 7400 series, they use NPN or pnp bipolar junction transistors.*
b. CMOS (Complementary Metal-Oxide-Silicon) i.e. 4000 series, they use complementary MOSFET or JFET type Field Effect Transistors.

There are 7 logic gates with whose help digital circuits are constructed. They are:
a. AND
b. OR
c. NOT
d. NAND
e. NOR
f. Ex-OR
g. Ex-NOR

In digital design only two voltage levels or states are allowed and these states are generally referred to as logic"1" high (true) and logic "0" low (false). These two states are represented in truth tables by the binary digits of"1" and "0" respectively.

Most digital logical circuits use "Positive logic" in which a logic level "0" or "LOW" is represented by a zero voltage, 0v or ground and a logic level "1" or "HIGH" is represented by a higher voltage such as +5 volts; but there exist "Negative Logic" also in which the values and the rules are reversed.

AND Gate:

The AND gate is an electronic circuit that gives a **high** output (1) only if all its inputs are high otherwise the output will remain "off". A dot (.) is used to show the AND operation i.e. A.B. it is used with two or more switches or other inputs

Table 1: AND gate symbol

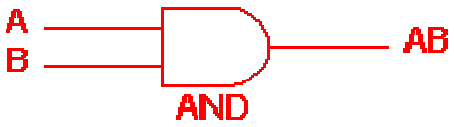


Table 2: AND gate truth table

2 Input AND gate		
A	B	A.B
0	0	0
0	1	0
1	0	0
1	1	1

OR Gate

The OR gate is an electronic circuit that gives a high output (1) if **one or more** of its inputs are high. A plus (+) is used to show the OR operation. They have two bit of input and a single bit of output.

Table 3: OR gate symbol

Table 4: OR gate truth table

2 Input OR gate		
A	B	A+B
0	0	0
0	1	1
1	0	1
1	1	1

NOT Gate

It is an electronic circuit that produces an inverted version of the input at its output and is also called as an inverter. If the input variable is A, the inverted output is known as NOT A. This is also shown as A', or A with a bar over the top. It has a single bit input and a single bit of output. The circle on the right of the triangle indicates the "negation".

Table 5: NOT gate symbol

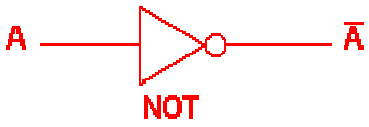


Table 6: NOT gate truth table

NOT gate	
A	$\overline{A}$
0	1
1	0

The diagrams below show two ways that the NAND logic gate can be configured to produce a NOT gate

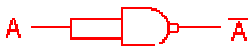


Table 7: Not using NAND

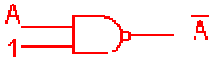


Table 8: NOT using NOR

It can also be done using NOR logic gates in the same way.

NAND Gate

This is a NOT-AND gate which is equal to an AND gate followed by a NOT gate i.e. it is opposite to the AND gate. The outputs of all NAND gates are high if **any** of the inputs are low. The symbol is an AND gate with a small circle on the output. The small circle represents inversion .the gate requires two or more bit of inputs and a single bit of output. The functions implemented y NAND gate is that it is symmetric as well as not associative.

Table 9: NAND gate symbol

Table 10: NAND gate truth table

2 Input NAND gate		
A	B	$\overline{A.B}$
0	0	1
0	1	1
1	0	1
1	1	0

NOR Gate

This is a NOT-OR gate which is equal to an OR gate followed by a NOT gate i.e. opposite of the OR gate. The outputs of all NOR gates are low if any of the inputs are high. The symbol is an OR gate with a small circle on the output. The small circle represents inversion. It has two bits of input and a single bit of output. The functions implemented by NOR gate is that it is symmetric and is not associative.

Table 11: NOR gate symbol

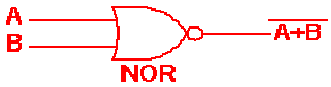


Table 12: NOR gate truth table

2 Input NOR gate		
A	B	$\overline{A+B}$
0	0	1
0	1	0
1	0	0
1	1	0

EX-OR GATE

The 'Exclusive-OR' gate is a circuit which will give a high output if either, but not both, of its two inputs are high because of this property, XOR gates are commonly found in complex

Redstone circuits. An encircled plus sign (⊕) is used to show the EOR operation. It has two bit of input and a single bit of output. If you look closely at the drawing of the gate we will see that, there is a second arc behind the first one near the inputs which is hard to see and thus XOR is usually written inside the gate. The function implemented by XOR gate has interesting properties such as the function is symmetric and also that the function is associative.

Table 13: EX-OR gate symbol

Table 14: EX-OR gate truth table

2 Input EXOR gate		
A	B	A⊕B
0	0	0
0	1	1
1	0	1
1	1	0

EX-NOR Gate

The **'Exclusive-NOR'** gate circuit does the opposite to the EOR gate. It will give a low output if either, but not both, of its two inputs are high. The symbol is an EXOR gate with a small circle on the output. The small circle represents inversion. They have two bits of input and a single bit of output. . If you look closely at the drawing of the gate we will see that, there is a second arc behind the first one near the inputs which is hard to see and thus XNOR is usually written inside the gate. The function implemented by XNOR gate has properties such as it is symmetric and also that it is associative.

Table 15: EX-NOR gate symbol

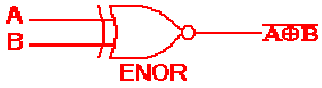
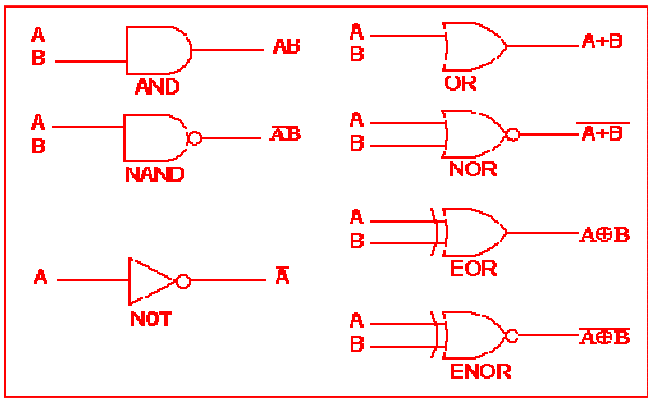


Table 16: EX-NOR gate symbol

2 Input EXNOR gate		
A	B	$\overline{A \oplus B}$
0	0	1
0	1	0
1	0	0
1	1	1

The NAND and NOR gate are called universal functions as with either one the AND and OR functions and NOT can be generated. A function in *sum of products* form can be implemented using NAND gates by replacing all AND and OR gates by NAND gates. A function in *product of sums* form can be implemented using NOR gates by replacing all AND and OR gates by NOR gates.

Table 17: A summary of few logic gates discussed above



A summary of the truth table of the input/output combinations for the NOT gate together with all possible input/output combinations for the other gate functions is given by:

Table 17: summary of logic gate truth table discussed above:

NOT gate	
A	$\overline{A}$
0	1
1	0

INPUTS		OUTPUTS					
A	B	AND	NAND	OR	NOR	EXOR	EXNOR
0	0	0	1	0	1	0	1
0	1	0	1	1	0	1	0
1	0	0	1	1	0	1	0
1	1	1	0	1	0	0	1

Half Adder

Adder circuit is a combinational digital circuit that is used for adding two numbers. A typical adder circuit produces a sum bit (denoted by S) and a carry bit (denoted by C) as the output. If A and B are the input bits, then sum bit (S) is the X-OR of A and B and the carry bit (C) will be the AND of A and B. Half adder is the simplest of all adder circuit, but it has a major disadvantage. The half adder can add only two input bits (A and B) and has nothing to do with the carry if there is any in the input. So if the input to a half adder have a carry, then it will be neglected it and adds only the A and B bits. That means the binary addition process is not complete and that's why it is called a half adder.

Table 18: circuit diagram of Half Adder

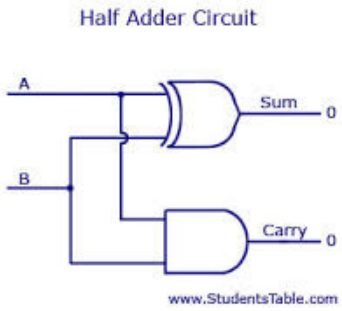


Table 19: truth table of Half Adder

A	B	S	C
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Full Adder

This type of adder is a little more difficult to implement than a half-adder. The main difference between a half-adder and a full-adder is that the full-adder has three inputs and two outputs. The first two inputs are A and B and the third input is an input carry designated as CIN. When full adder logic is designed we will be able to string eight of them together to create a byte-wide adder and cascade the carry bit from one adder to the next.

The output carry is designated as COUT and the normal output is designated as S. We can see that the output S is an EXOR between the input A and the half-adder SUM output with B and CIN inputs. We must also note that the COUT will only be true if any of the two inputs out of the three are HIGH. We can see that the output S is an EXOR between the input A and the half-adder SUM output with B and CIN inputs. We must also note that the COUT will only be true if any of the two inputs out of the three are HIGH.

Table 20: circuit diagram of full adder

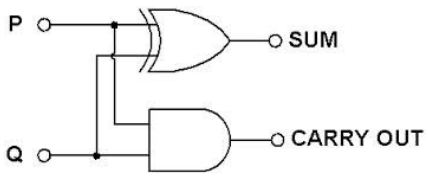


Table 21: truth table of full adder

Full Adder –Truth Table				
Input			Output	
A	B	Carry in	Sum	Carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1
www.flintgroups.com				

Half Subtractor

Half Subtractor is a combinational circuit that performs subtraction of two bits and has two inputs and two outputs. The two inputs denoted by A and B represents minuend and subtrahend. The two outputs are the difference "D" and the borrow bit "B_o". From the truth table, Boolean Expression can be derived as:

D = A'B + AB' = $A \oplus B$

B_o = A'B

A Half Subtractor circuit can be implemented using AND & OR logic gates or by using XOR, NOT & AND logic gates.

Table 22: circuit diagram of half subtractor.

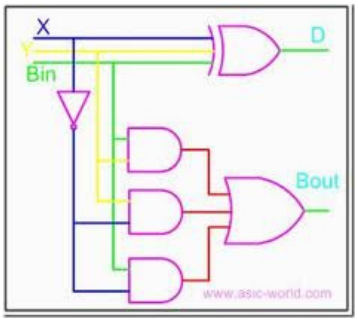


Table 23: truth table of half subtractor

Half Subtractor-Truth Table			
Input		Output	
A	B	Difference	Borrow
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0
www.flintgroups.com			

Full Subtractor

As in the case of the addition using logic gates, a *full subtractor* is made by combining two half-subtractor and an additional OR-gate. A full subtractor has the borrow in capability (denoted as BOR_{IN} in the diagram below) and so allows *cascading* which results in the possibility of multi-bit subtraction

= X'Y'Bin + X'YBin' + XY'Bin' + XYBin
= (X'Y' + XY)Bin + (X'Y + XY')Bin'
= (X ⊕ Y)'Bin + (X ⊕ Y)Bin'
= X ⊕ Y ⊕ Bin
Bout = X'.Y + X'.Bin + Y.Bin

Table 24: circuit diagram of full subtractor

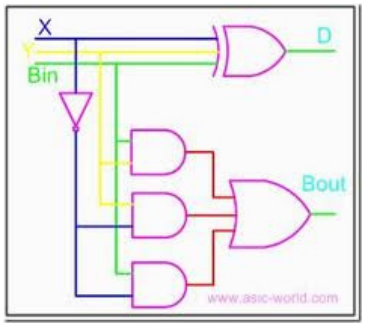


Table 25: Truth table of Full Subtractor

Full Subtractor-Truth Table				
Input			Output	
A	B	C	Difference	Borrow
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1
www.flintgroups.com				

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